TPS74701EVM-177 and TPS74801EVM-177

This user's guide describes the characteristics, operation, and use of the TPS74x01EVM-177 evaluation module (EVM). This EVM contains either the TPS74701 or TPS74801 low-dropout linear regulator IC. This user's guide includes EVM specifications, recommended test setup, test results, bill of materials (BOM), and a schematic diagram.

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1 Introduction

The Texas Instruments TPS74x01EVM-177 evaluation module uses the TPS74701 or TPS74801 low-dropout linear regulator IC. These regulators require a low-power bias voltage, V_{BIAS}, and a power input voltage, V_{IN}. These two regulators are capable of providing output voltages down to 0.8 V and have an integrated supervisory circuit with open-drain output that goes to high impedance when the output voltage reaches regulation (power good or PG). The TPS74701 and TPS74801 can provide up to 0.5 A and 1.5 A of output current, respectively, and each has a soft start (SS) pin which allows the user to set the output voltage's linear ramp rate at startup. The goal of the EVM is to facilitate evaluation of the TPS74x01 ICs.

1.1 *Performance Specification Summary*

Table 1 provides a summary of the TPS74x01EVM-177 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

	CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
		MIN	TYP	MAX	MIN	TYP	MAX
V_{BIAS} supply	TPS74801EVM-177 (HPA177-001), V_{IN} = V_{BIAS}, I_{OUT} = 1.5A	2.83[(1)]	5	5.5		5	
	TPS74701EVM-177 (HPA177-002), V_{IN} = V_{BIAS}, I_{OUT} = 0.5A	2.7[(1)]	5	5.5		5	
V_{IN} supply	TPS74801EVM-177 (HPA177-001), V_{BIAS} - V_{OUT} ≥ 3.25 V, I_{OUT} = 1.5A	1.395[(1)]		5.5[(2)]			1500
	TPS74701EVM-177 (HPA177-002), V_{BIAS} - V_{OUT} ≥ 1.62 V, I_{OUT} = 0.5A	1.35[(1)]		5.5[(2)]			500
V_{OUT}	TPS74801EVM-177 (HPA177-001)	1.17[(3)]	1.20	1.23[(3)]			1500[(2)]
V_{OUT}	TPS74701EVM-177 (HPA177-002)	1.17[(3)]	1.20	1.23[(3)]			500[(2)]

(1) This is the minimum voltage to provide the maximum output current in the table assuming the typical V_{BIAS} voltage is applied. Lower output currents are achievable with lower V_{IN} and V_{BIAS} voltages. See the data sheet for V_{IN} to V_{OUT} and V_{BIAS} to V_{OUT} dropout data.

(2) Linear regulator power dissipation is computed as $P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$. As specified in the data sheet, the regulator's package has a finite power dissipation rating depending on the ambient temperature, board type, and airflow. Using V_{IN} and/or V_{OUT} voltages other than the typical voltages recommended in the table or using the EVM in an environment with an ambient temperature higher than 25°C significantly reduces the maximum allowed output current. See the data sheet for the regulator package's thermal resistance data, and see TI application report *Digital Designer's Guide to Linear Voltage Regulators and Thermal Management* (SLVA118) for a full explanation.

(3) The EVM uses ±1% feedback resistors. Therefore, the EVM output tolerance is the ±2% internal reference tolerance plus $2 \times (1 – V_{REF}/V_{OUT}) \times TOL_{FBRES}$ = 2 × (1– 0.8 V/1.2 V) × ±1% = 0.67% or ±2.67%. For tighter output tolerance, tighter tolerance feedback resistors must be used.

1.2 *Modifications*

To aid user customization of the EVM, the board was designed with devices having 0603 or larger footprints. A real implementation likely occupies less total board space.

Changing components can improve or degrade EVM performance. For example, adding a larger output capacitor reduces output voltage undershoot but lengthens response time after a load transient event. Adding a larger input capacitor reduces droop at the V_{IN} pin that inductive leads from the V_{IN} power supply may cause during a load transient.

2 Input/Output Connector Descriptions

J1–VIN/GND This terminal block has both a positive and ground return connection to the power input (V_{IN}) supply. The leads to the input supply should be twisted and kept as short as possible.

J2–GND This header is the return connection for the bias (V_{BIAS}) supply.

J3–VIN This header is a positive connection to the power input supply (V_{IN}). Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1A$) evaluation or as a voltage test point.

J4–VBIAS This header is the positive connection for the bias (V_{BIAS}) supply.

J5–GND This header is a ground return connection to the power input (V_{IN}) supply. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1A$) evaluation or as a ground test point.

J6–VOUT This header is the positive connection for the output load on V_{OUT}. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1A$) evaluation only or as a voltage test point.

J7–GND This header is the ground return connection for the output load. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1A$) evaluation or as a ground test point.

J8–VOUT/GND This terminal block has both a positive and ground return connection for the output load. The leads to the output load should be twisted and kept as short as possible.

J9–TRACK IN This header is not populated on the TPS74701 or TPS74801 EVMs.

J10–EN This header is a connection to the enable pin (EN), which is also connected to the middle pin of S1. When S1 is OFF, the EN pin is pulled to ground through pull-down resistor. When applying an external signal to drive EN, S1 should in the OFF position.

J11–GND This header is a ground connection.

JP1– 1ms/Simult vs. 10ms/Ratio For the TPS74701 and TPS74801, this jumper allows the user to choose either 1 ms or 10 ms soft start time for the output voltage. Leaving the jumper open results in the output voltage ramping up with default soft-start time of 500 us.

S1 - This switch connects to the EN pin of the IC and allows the user to turn the IC ON or OFF by connecting enable to either V_{BIAS} or ground through a pull-down resistor.

TP1 - This is a Kelvin test point to V_{IN}.

TP2 - This is a Kelvin test point to IC ground.

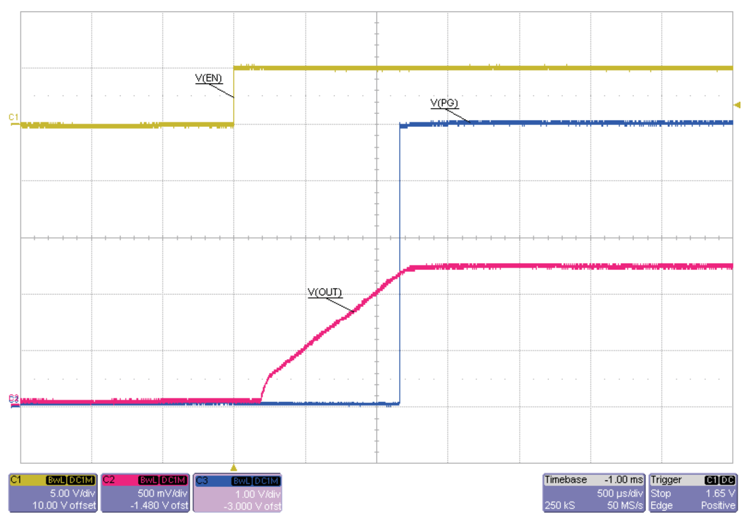
TP3 - This is a Kelvin test point to V_{OUT}.

2.1 Test Setup

The absolute maximum voltage allowed on the BIAS, IN, or EN pins is 6 V. The TPS74701 and TPS74801 devices are designed to operate with V_{IN} and V_{BIAS} less than or equal to 5.5 V. To enable the regulator, switch S1 to the ON position. When connecting external loads, use short, twisted leads in order to minimize DC drop at the connector and/or inductive voltage dip after a transient load is removed.

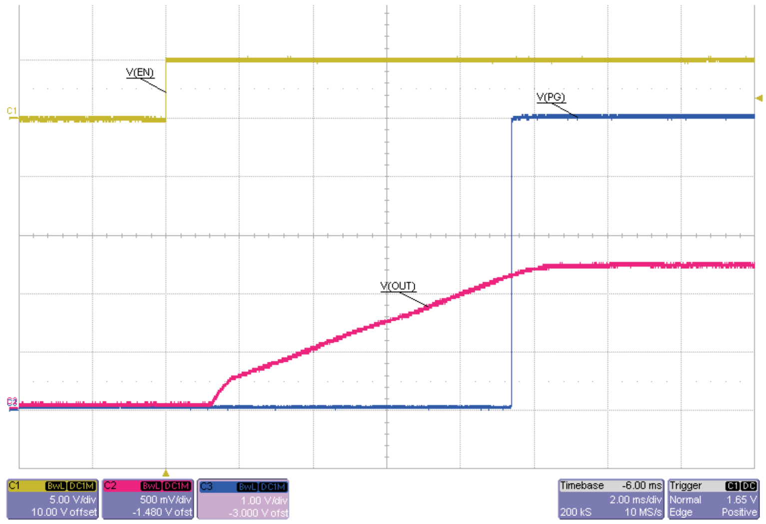
2.2 Test Results

The figures below show the test results at T_A = 25°C using this EVM:



A V_{IN} = 1.8 V, V_{BIAS} = 5.0 V, I_{OUT} = 500 m A.

Figure 1. TPS74701 and TPS74801 Start-up in 1 mS with PG



A V_{IN} = 1.8 V, V_{BIAS} = 5.0 V, I_{OUT} = 500 mA.

Figure 2. TPS74701 and TPS74801 Start-up in 10 mS with PG

3 Board Layout

Board layout is important for best PSR and lowest noise. Figure 3, Figure 4, and Figure 5 show the board layout for the HPA177 PWB. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry, and careful attention has been given to the routing of high-frequency current loops. See the data sheet for more specific layout guidelines.

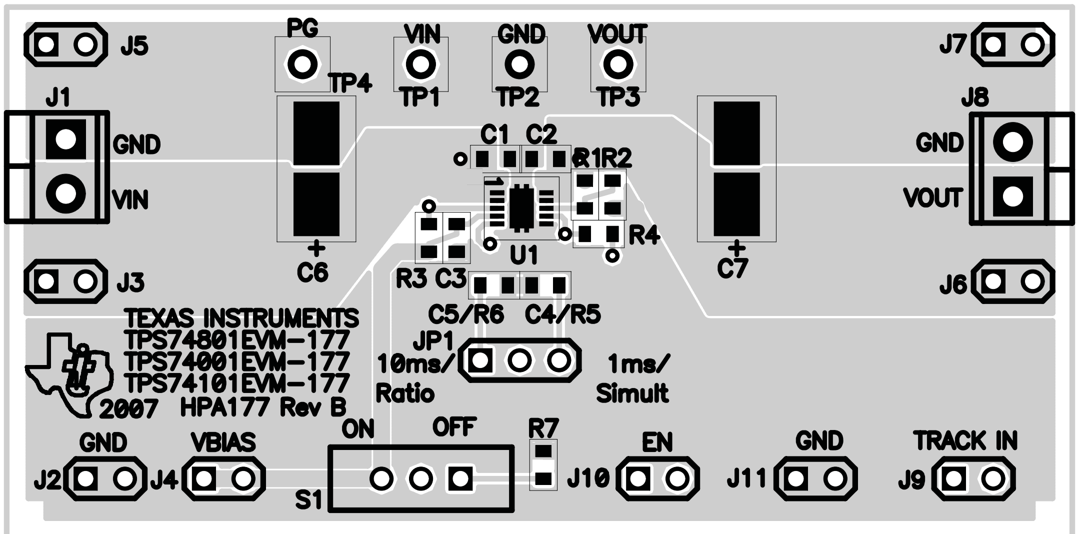


Figure 3. Top Assembly Layer

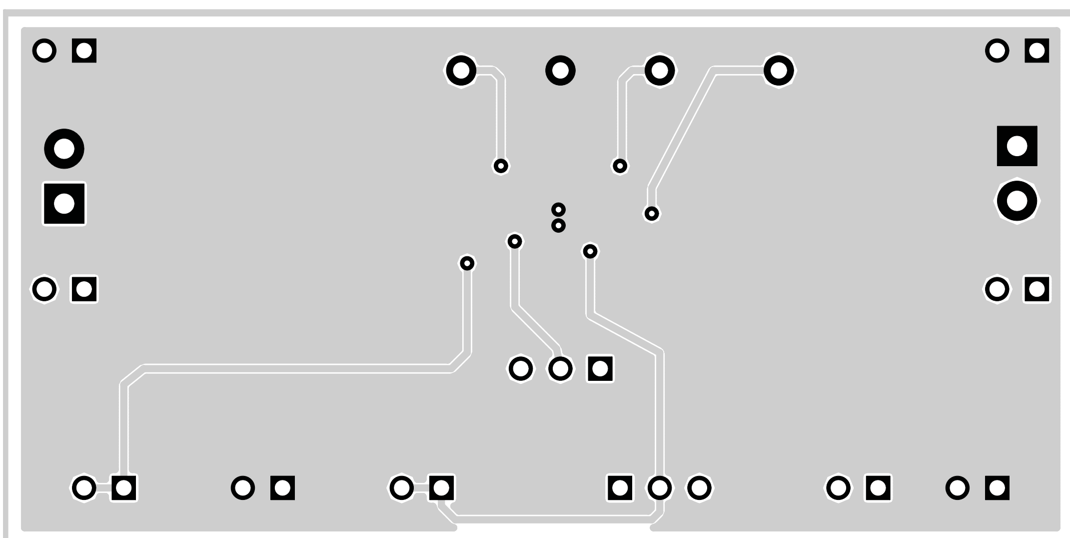


Figure 4. Top Layer

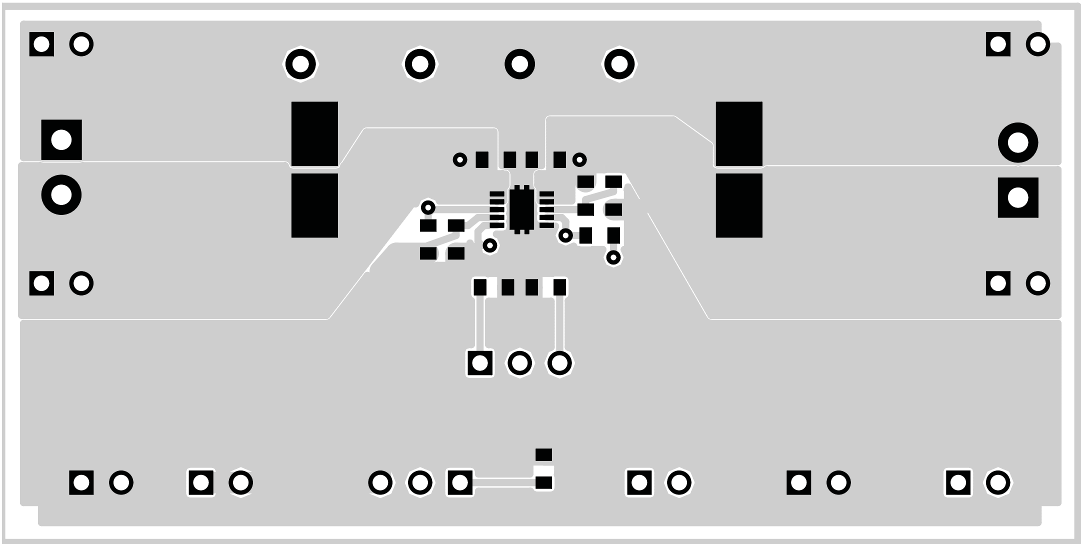


Figure 5. Bottom Layer

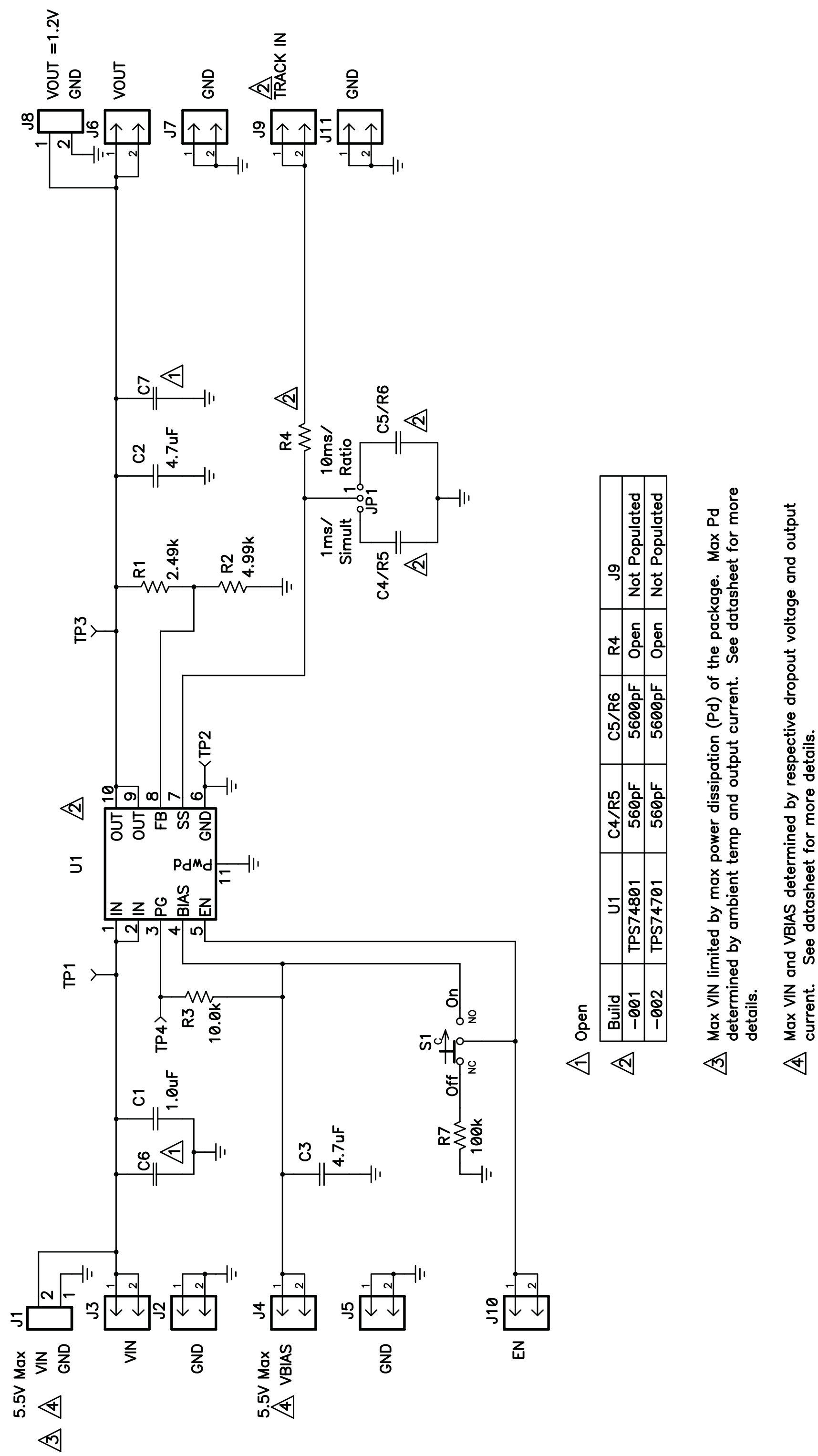
4 Bill of Materials and Schematic

Table 5. HPA177 Bill of Materials

COUNT							
-001	-002	RefDes	Value	DESCRIPTION	SIZE	Part Number	MFR
2	2	C1	1.0uF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK
2	2	C3, C2	4.7uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C1608X5R0J475K	TDK
1	1	C4	560pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H561J	TDK
1	1	C5	5600pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	GRM188R71H562KA01D	muRata
0	0	C6, C7	Open	Capacitor, Multi-pattern, 603-D case	7343 (D)		
2	2	J1**, J8** J2 - J7, J10,		Terminal Block, 2 pin, 6A, 3.5mm	0.27 x 0.25	ED1514	OST
8	8	J11		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
0	0	J9		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
1	1	JP1		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
1	1	R1	2.49k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	R2	4.99k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	R3	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	R4	4.99k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	R5	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	R6	1.78k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	R7	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	S1		Switch, 1P2T, Slide, PC mount, 200mA	0.46 x 0.16	EG1218	E_Switch
3	3	TP1, TP3, TP4		Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100	5000	Keystone
1	1	TP2		Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100	5001	Keystone
1	0	U1		IC, 1.5A LDO Regulator with Soft-Start	SON-10	TPS74801DRC	TI
0	1			IC, 500mA LDO With Programmable Soft Start	SON-10	TPS74701DRC	TI
1	1	--		PCB, 2.7 In x 1.345 In x 0.062 In		HPA177	Any
1	1	--		Shunt, 100mil, Black	0.100	929950-00	

5.1 Schematic Drawing

Figure 6 is the schematic for the TPS74x01EVM-177.



Build	U1	C4/R5	C5/R6	R4	J9
−001	TPS74801	560pF	5600pF	Open	Not Populated
−002	TPS74701	560pF	5600pF	Open	Not Populated

Figure 6. Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 5 V and the output voltage range of 3 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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